Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the present application:

Listing of the Claims:

1-16. (Canceled).

17. (Original) An integrated circuit device comprising:

an integrated circuit substrate;

an interlayer dielectric on the integrated circuit substrate having a plurality of buried contacts therein;

an oxide layer on the interlayer dielectric;

an intaglio pattern in the oxide layer over the buried contacts; and

a plurality of lower electrodes within a single opening in the intaglio pattern, the lower electrodes electrically contacting corresponding ones of the buried contacts.

18. (Original) The integrated circuit device of Claim 17 wherein the lower electrodes comprise semi-cylindrical lower electrodes symmetrically arranged in the intaglio pattern.

19. (Original) The integrated circuit device of Claim 17 wherein the integrated circuit device comprises a ferroelectric memory device and wherein the lower electrodes are lower electrodes of capacitors, the capacitors further comprising a ferroelectric layer on the lower electrodes and upper electrodes on the ferroelectric layers.

20. (Original) The integrated circuit device of Claim 19 wherein at least one of the lower electrodes comprises:

a horizontal electrode component contacting an upper surface of its corresponding buried contact; and

a vertical electrode component extending from the horizontal electrode component on a sidewall of the intaglio pattern.

21. (Original) The integrated circuit device of Claim 19 further comprising a plurality of transistors in the integrated circuit substrate and wherein the buried contacts electrically contact corresponding ones of the transistors.

22. (Original) The integrated circuit device of Claim 19 wherein the intaglio pattern comprises a multi-step intaglio pattern extending along upper surfaces of the buried contacts and a part of inner sidewalls of the buried contacts.

23. (Original) The integrated circuit device of Claim 22 wherein at least one of the lower electrodes comprises:

a first vertical electrode component extending along the part of the inner sidewall of its corresponding buried contact;

a horizontal electrode component extending from the first vertical electrode component along the upper surface of its corresponding buried contact; and

a second vertical electrode component extending from the horizontal electrode component along a sidewall of the multi-step intaglio pattern in the oxide layer.

24. (Original) The integrated circuit device of Claim 23 wherein the at least one of the lower electrodes further comprises a second horizontal electrode component extending inwardly from the first vertical electrode along a surface of the interlayer dielectric lower than a surface of the interlayer dielectric beyond the buried contacts.

25. (Original) The integrated circuit device of Claim 22 wherein the capacitors comprise semi-cylindrical capacitors symmetrically arranged in the intaglio pattern.

26-29. (Canceled).

30. (Original) A ferroelectric memory device including semi-cylindrical capacitors, comprising:

an interlayer dielectric including at least two buried contacts;

an oxide layer formed on the interlayer dielectric;

an intaglio pattern exposing upper surfaces of the at least two buried contacts;

at least two lower electrodes formed in the intaglio pattern, each of the at least two lower electrodes being in contact with a corresponding one of the at least two buried contacts; and

a ferroelectric layer and an upper electrode sequentially formed on the lower electrodes.

31. (Original) A ferroelectric memory device including semi-cylindrical capacitors, comprising:

an interlayer dielectric including at least two buried contacts;

an oxide layer formed on the interlayer dielectric;

a two-step intaglio pattern exposing upper surfaces and a part of sidewalls of the at least two buried contacts;

at least two lower electrodes formed in the two-step intaglio pattern, each of the at least two lower electrodes being in contact with a corresponding one of the at least two buried contacts; and

a ferroelectric layer and an upper electrode sequentially formed on the lower electrodes.